

REMARKS

The examiner rejected claims 1 and 3-21 as being unpatentable over U.S. patent No. 6,212,542 to Kahle in view of U.S. Patent No. 6,373,848. The examiner identified the '848 patent as having been issued to Belkin. However, applicant notes that the '848 patent has in fact been issued to Allison et al., whereas the Belkin patent is U.S. Patent No. 6,604,125.

Applicant's independent claim 1 recites "scheduling a first thread provided by the multiple programmable multi-threaded engines integrated within the processor to process a first incoming block of data within a network packet received at port of a media access control device to move the first incoming block of data to a first location in a memory coupled to the processor." Thus, applicant's claim 1 uses processor threads to move incoming blocks of data received at a media access control (MAC device) to a memory coupled to the processor.

In contrast, none of the references cited by the examiner discloses or suggest "scheduling a first thread ... to process a first incoming block of data within a network packet received at port of a media access control device to move the first incoming block of data to a first location in a memory coupled to the processor," as required by applicant's independent claim 1. As it is not clear from the office action whether the examiner relied upon Belkin or Allison to support the rejection of the claims, applicant will consider both these references.

Kahle describes a multi-scalar data processor 100, and explains:

Still referring to FIG. 4, the execution circuitry of multi-scalar processor 100 includes thread scheduler 130 and a scalable number of identical processing elements (PEs), which in the illustrative embodiment include PEs 132, 134, 136, and 138. In accordance with the multi-scalar software architecture described above, thread scheduler 130 processes thread descriptors within the T-Code stream of a multi-scalar program in order to assign multiple threads to PEs 132-138 for concurrent execution. In order to reduce access latency, thread scheduler 130 is equipped with a T-Code cache 44 that stores the thread descriptors, thereby establishing separate fetch paths for the I-Code and T-Code streams. As noted above, ordinarily only one of PEs 132-138 executes non-speculatively at a time. The non-speculative thread, which is the earliest occurring thread in program order among the executing threads (and the thread that contains the instruction to which IP 126 points), is indicated by thread pointer (TP) 142 maintained by thread scheduler 130. (Emphasis added, Kahle, col. 10, line 57, to col. 11, line 8)

While Kahle describes a thread scheduler that assigned threads to PEs 132-138 for concurrent execution, at no point does Kahle describe scheduling threads to process blocks of data to move those blocks of data from a MAC device to a memory location. Indeed, as admitted by the examiner, Kahle does not describe any type of network, or network data processing, and Applicant contends Kahle in fact does not describe a media access control device. Accordingly, Kahle fails to disclose or suggest at least the features of “scheduling a first thread … to process a first incoming block of data within a network packet received at port of a media access control device to move the first incoming block of data to a first location in a memory coupled to the processor,” as required by applicant’s independent claim 1.

The examiner uses Belkin (US 6,604,125) (or Alison) to teach “**…using a processor having multiple thread engines to process network data.**” (see Final Action, page 3).

Belkin (US 6,604,125) describes a mechanism for enabling a thread unaware or non-thread-safe application to be executed safely in a multi-threaded environment (Belkin, col. 1, lines 15-18). Particularly Belkin describes using threads to service requests¹. But Belkin does not describe that threads are used to processing incoming network data received in a MAC device to move the data from the MAC device to a memory coupled to the processor. Indeed, Belkin does not at all discuss MAC devices. Accordingly, Belkin too fails to disclose or suggest at least the features of “scheduling a first thread … to process a first incoming block of data within a network packet received at port of a media access control device to move the first incoming block of data to a first location in a memory coupled to the processor,” as required by applicant’s independent claim 1.

Allison describes a multi-port adapter having a single MAC serving all ports (Allison, col. 1, lines 17-18). While Allison describes transmit and receive functionality of a multi-port adapter, at no point does Allison suggest the transfer of data to a processor memory. Allison also does not at all discuss the use of threads, and certainly does not discuss the use of threads to move incoming blocks of data received at the Allison’s interface to a memory coupled to a processor. Accordingly, Allison also fails to disclose or suggest at least the features of

¹ See, for example, Belkin, col. 5, lines 27-63.

“scheduling a first thread … to process a first incoming block of data within a network packet received at port of a media access control device to move the first incoming block of data to a first location in a memory coupled to the processor,” as required by applicant’s independent claim 1.

Because none of Kahle, Belkin and/or Allison discloses or suggests, alone or in combination, at least the features of “scheduling a first thread … to process a first incoming block of data within a network packet received at port of a media access control device to move the first incoming block of data to a first location in a memory coupled to the processor,” applicant’s independent claim 1, and the claims depending from it, are patentable over the cited art.

Applicant’s independent claims 7 and 15 recite “processing a first portion of the network packet received at port of a media access control device using a first thread provided by the multiple programmable multi-threaded engines integrated within the processor to move the first portion of the network packet to a first location in a memory coupled to the processor,” or similar language. For reasons similar to those provided with respect to independent claim 1, at least these features are not disclosed by the cited art. Accordingly, applicant’s claims 7 and 15, and the respective claims depending from them, are patentable over the cited art.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

In view of the foregoing, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner’s earliest convenience.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner’s positions with respect to that claim or other claims.

Enclosed is a Request for Continued Examination.

Applicant : Donald F. Hooper, et al.
Serial No. : 09/626,535
Filed : July 27, 2000
Page : 9 of 9

Attorney's Docket No.: 10559-137002 / P7876X

The fees in the amount of \$810 are being paid concurrently on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other required fees to deposit account 06-1050, referencing the attorney docket number shown above.

Respectfully submitted,

Date: Oct. 22, 2007



Ido Rabinovitch
Attorney for Intel Corporation
Reg. No. L0080

Customer No. 20985
Fish & Richardson P.C.
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

21749069.doc